ABSTRACT OF THE DISCLOSURE

A self aligned method of forming a semiconductor memory array of floating gate memory cells in a semiconductor substrate has a plurality of spaced apart isolation regions and active regions on the substrate substantially parallel to one another in the column direction. Floating gates are formed in each of the active regions by forming a conductive layer of material. Trenches are formed in the row direction across the active regions, and are filled with a conductive material to form blocks of conductive material that are the control gates. Sidewall spacers of conductive material are formed along the floating gate blocks to give the floating gates protruding portions that extend over the floating gate.

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